Northern University Bangladesh



**Lab report:** 02

**Department:** CSE

**Course title:** Digital Electronics & Pulse Technique Lab Work

**Experiment no:** CSE 2366

**Experiment name:** Implement Diode Register Logic AND, OR and NOT gate in Tinkercad

**Submitted by** **Submitted to**

Name of teacher: Nizia Nahyan

Designation: Lecturer

Signature:

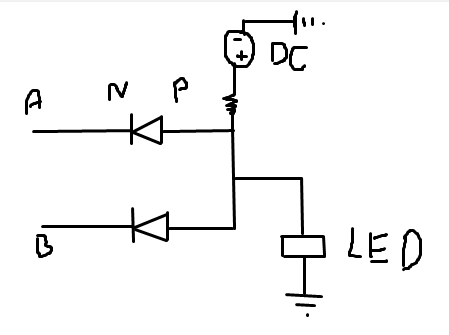
Name: Fardeen Ahmed

Id: 41210301615

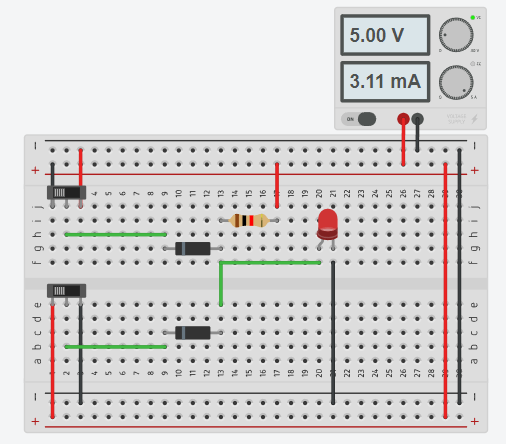
Date of Experiment: 10/6/2024

Date of submission: 22/6/2024

DRL AND gate

Circuit diagram:

Circuits Screenshot:

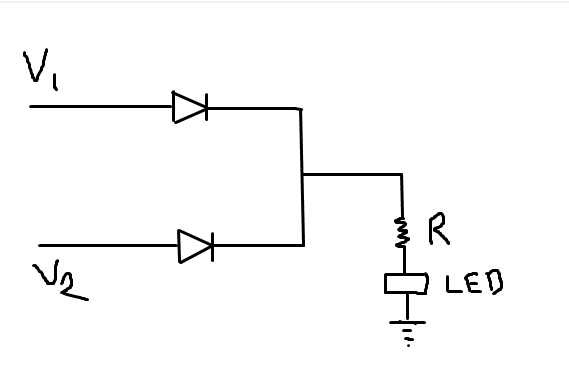


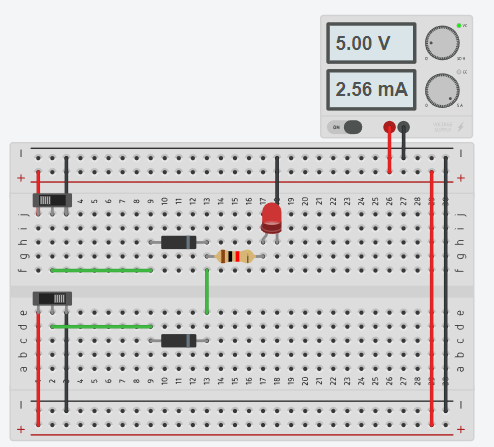
Tinkercad circuit link:

<https://www.tinkercad.com/things/0M60e5Ftp00-drl-and-gate-1615?sharecode=U_oHK8NgMZTldVPNzLoqu8tAqYxAOJa_li8h34nqDsg>

DRL OR gate

Circuit diagram:



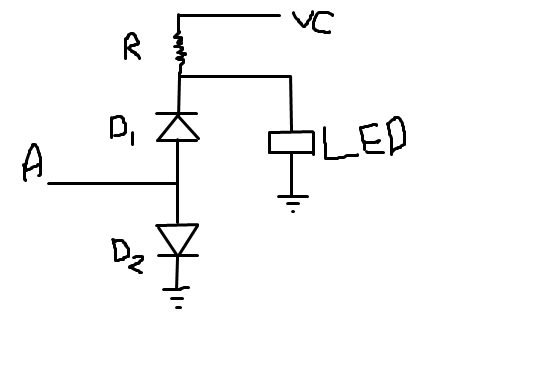
Circuit screenshot:

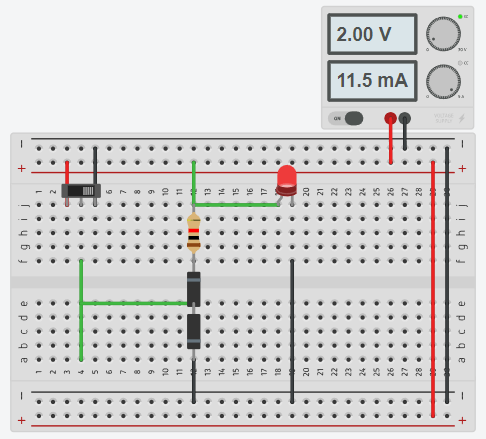
Tinkercad circuit link:

<https://www.tinkercad.com/things/37vQ5VAtfZG-drl-or-gate-1615?sharecode=SsDHrRljnQ_2Fh0d1eu62u5WvcSm0xFriwkUzojUw_M>

DRL NOT gate

Circuit diagram:



Circuit screenshot:

Tinkercad circuit link:

<https://www.tinkercad.com/things/dTpGLXZBjav-drl-not-gate-1615?sharecode=jBjhTpjTsVocOSnPafBePKY6huXse9GyyWZn5rx9Fnw>